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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	FIRST NAMED INVENTOR ATTORNEY DOCKET NO.	
10/698,727	10/31/2003	Matthew L. Seidl	SUN-P9719-SPL	1586
22835	7590 01/12/2006		EXAMINER	
	RD PARK, REG. NO. 4 JGHAN & FLEMING LI	MOORE, PATRICK M		
2820 FIFTH		ART UNIT	PAPER NUMBER	
DAVIS, CA	95616		2188	
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Please find below and/or attached an Office communication concerning this application or proceeding.

		1	Application No.	Applicant(s)			
Office Action Summary			10/698,727	SEIDI ET AL.			
		E	Examiner	Art Unit			
		F	Patrick M. Moore	2188			
	- The MAILING DATE of this communication appears on the cover sheet with the correspondence address - Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
1)🖂	Responsive to communication(s) filed on <u>31 October 2003</u> .						
2a) <u></u> □	This action is FINAL . 2b)⊠ This action is non-final.						
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
 4) Claim(s) 1-21 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-21 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. 							
Applicati	on Papers		•				
9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority under 35 U.S.C. § 119							
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
Attachment(s)							
1) Notic	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PT	-O 048)	4) Interview Summary Paper No(s)/Mail Da				
3) Inform	e of Dransperson's Patent Drawing Review (Pi nation Disclosure Statement(s) (PTO-1449 or F r No(s)/Mail Date			ratent Application (PTO-152)			

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DETAILED ACTION

Claims 1-21 have been examined

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Chopra et al. (US Patent # 6,412,043), herein referred to as Chopra.
 - a. As per Claim 1, Chopra discloses a method for supporting read-only objects within an object-addressed memory hierarchy, comprising: receiving a request to access an object, wherein the request includes an object identifier for the object that is used to reference the object within the object-addressed memory hierarchy [Figure 9, # 200 & Column 41, Lines 3-7]; using the object identifier to retrieve an object table entry associated with the object [Figure 9, # 212 & Column 41, Lines 23-24]; if the request is a write request [Column 41, Lines 3-4], examining a read-only indicator within the object table entry [Figure 9, # 212, 214 & Column 41, Lines 25-29], if the read-only indicator specifies that the object is a read-only object, performing a corrective action to deal with the fact that the write request is directed to a read-only object [Figure 9, # 218 & Column 41, Lines 31-35].

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b. As per Claim 2, Chopra further discloses the method of claim 1, wherein if the request is a read request, the method further comprises using a physical address from the object table entry to access the object in main memory [Figure 9, # 222, Figure 10, #248, Column 41, Lines 53-59 & Column 42, Lines 34-40].

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- c. As per Claim 3, Chopra further discloses the method of claim 1, wherein performing the corrective action can involve causing a fault handler in the requesting processor to perform the corrective action [Figure 9, # 218 & Column 41, Lines 31-35].
- d. As per Claim 4, Chopra further discloses the method of claim 1, wherein performing the corrective action can involve: obtaining a writable copy of the object, clearing the read-only indicator to indicate that the object is no longer read-only, and updating the writable copy of the object with data from the write request [Column 17, Lines 4-20]; updating a remotely located master copy of the object with data from the write request [Column 27, Lines 48-55]; terminating the requesting process because the write request is not allowed [Column 43, Lines 41-55]; and if the request is directed to a debugging breakpoint, pausing the requesting process and clearing the read-only indicator [Column 14, Lines 42-59].
- e. As per Claim 5, Chopra further discloses the method of claim 1, wherein the request to access the object is received at a translator that translates between object identifiers (used to reference objects in an object cache) and

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physical addresses (used to address objects in main memory) [a "TLB" as defined in Column 1, Lines 22-24].

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- f. As per Claim 6, Chopra further discloses the method of claim 5, wherein prior to receiving the request at the translator, the request is initially directed to the object cache [Figure 9, #202, 204 & Column 41, Lines 4-8]; wherein if the request causes a hit in the object cache, the object is accessed in the object cache and the request is not sent to the translator ["Yes" branch of Figure 9, #204 & Column 41, Lines 10-15]; and wherein if the request causes a miss in the object cache, the request is sent to the translator ["No" branch of Figure 9, #204 & Column 41, Lines 9-10].
- g. As per Claim 7, Chopra further discloses the method of claim 6, further comprising making a given object read-only by: setting a read-only indicator associated with the given object to indicate that the given object is read-only ["first instruction" in Column 46, Line 56]; causing all object caches within a local cache-coherent domain to flush any modified cache lines of the given object out to main memory ["first operation" in Column 46, Line 48]; whereby subsequent upgrades of the given object from read-only status to writable or modified status in any caches within the local cache-coherent domain must go through a translator [Column 47, Lines 8-14].
- h. As per Claim 8, Chopra further discloses the method of claim 7, wherein causing all object caches within the local cache-coherent domain to flush any modified cache lines of the given object out to main memory involves executing a

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read-with-intent-to-only-read (RWITOR) instruction on each cache line of the given object [Column 19, Lines 35-47]. Chopra defines a "SYNCO" instruction to function as a special flush mechanism, which dumps cache objects to main memory.

- i. As per Claim 9, Chopra further discloses the method of claim 7, wherein the given object can be made read-only in response to a request received from outside the local cache-coherent domain [Column 44, Lines 17-40].
- j. As per Claim 10, Chopra further discloses the method of claim 5, wherein the translator includes hardware to translate between object identifiers and physical addresses [Figure 1, # 110].
- k. As per Claim 11, Chopra discloses an apparatus that supports read-only objects within an object-addressed memory hierarchy, comprising: a receiving mechanism configured to receive a request to access an object, wherein the request includes an object identifier for the object that is used to reference the object within the object-addressed memory hierarchy [Figure 9, # 200 & Column 41, Lines 3-7]; a translation mechanism configured to use the object identifier to retrieve an object table entry associated with the object [Figure 9, # 212 & Column 41, Lines 23-24]; and a corrective action mechanism, wherein if the request is a write request [Figure 1, # 218 & Column 41, Lines 31-35], the corrective action mechanism is configured to, examine a read-only indicator within the object table entry [Figure 9, # 212, 214 & Column 41, Lines 25-29], and if the read-only indicator specifies that the object is a read-only object, to perform

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a corrective action to deal with the fact that the write request is directed to a read-only object [Figure 1, # 218 & Column 41, Lines 31-35].

- I. As per Claim 12, Chopra further discloses the apparatus of claim 11, wherein if the request is a read request, the translation mechanism is additionally configured to use a physical address from the object table entry to access the object in main memory [Figure 9, # 222, Figure 10, #248, Column 41, Lines 53-59 & Column 42, Lines 34-40].
- m. As per Claim 13, Chopra further discloses the apparatus of claim 11, wherein the corrective action mechanism is configured to cause a fault handler in the requesting processor to perform the corrective action [Figure 9, # 218 & Column 41, Lines 31-35].
- n. As per Claim 14, Chopra further discloses the apparatus of claim 11, wherein performing the corrective action can involve: obtaining a writable copy of the object, clearing the read-only indicator to indicate that the object is no longer read-only, and updating the writable copy of the object with data from the write request [Column 17, Lines 4-20]; updating a remotely located master copy of the object with data from the write request [Column 27, Lines 48-55]; terminating the requesting process because the write request is not allowed [Column 43, Lines 41-55]; and if the request is directed to a debugging breakpoint, pausing the requesting process and clearing the read-only indicator [Column 14, Lines 42-59].

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o. As per Claim 15, Chopra further discloses the apparatus of claim 11, wherein the receiving mechanism and the translation mechanism reside within a translator that translates between object identifiers (used to reference objects in an object cache) and physical addresses (used to address objects in main memory) [a "TLB" as defined in Column 1, Lines 22-24].

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- p. As per Claim 16, Chopra further discloses the apparatus of claim 15, wherein the apparatus includes the object cache; wherein prior to receiving the request at the translator, the request is initially directed to the object cache [Figure 9, #202, 204 & Column 41, Lines 4-8]; wherein if the request causes a hit in the object cache, the object is accessed in the object cache and the request is not sent to the translator ["Yes" branch of Figure 9, # 204 & Column 41, Lines 10-15]; and wherein if the request causes a miss in the object cache, the request is sent to the translator ["No" branch of Figure 9, # 204 & Column 41, Lines 9-10].
- q. As per Claim 17, Chopra further discloses the apparatus of claim 16, further comprising a read-only configuration mechanism configured to make a given object read-only by: setting a read-only indicator associated with the given object to indicate that the given object is read-only ["first instruction" in Column 46, Line 56]; causing all object caches within a local cache-coherent domain to flush any modified cache lines of the given object out to main memory ["first operation" in Column 46, Line 48]; whereby subsequent upgrades of the given object from read-only status to writable or modified status in any caches within

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the local cache-coherent domain must go through a translator [Column 47, Lines 8-14].

- r. As per Claim 18, Chopra further discloses the apparatus of claim 17, wherein the read-only configuration mechanism causes all object caches within the local cache-coherent domain to flush any modified cache lines of the given object out to main memory by executing a read-with-intent-to-only-read (RWITOR) instruction on each cache line of the given object [Column 19, Lines 35-47].
- s. As per Claim 19, Chopra further discloses the apparatus of claim 17, wherein the read-only configuration mechanism makes the given object read-only in response to a request received from outside the local cache-coherent domain [Column 44, Lines 17-40].
- t. As per Claim 20, Chopra further discloses the apparatus of claim 15, wherein the translator includes hardware to translate between object identifiers and physical addresses [Figure 1, # 110].
- u. As per Claim 21, Chopra discloses a computer system that supports readonly objects within an object-addressed memory hierarchy, comprising: a
 processor [Figure 1, # 100]; the object-addressed memory hierarchy [Figure 1, #
 102]; an object cache within the object-addressed memory hierarchy [Figure 1, #
 111]; a translator that translates between object identifiers, used to address
 objects in the object cache, and physical addresses, used to address objects in
 main memory [Figure 1, # 110]; a receiving mechanism within the translator

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configured to receive a request to access an object, wherein the request includes an object identifier for the object that is used to reference the object within the object-addressed memory hierarchy [Figure 9, # 200 & Column 41, Lines 3-7]; a translation mechanism within the translator configured to use the object identifier to retrieve an object table entry associated with the object [Figure 9, # 212 & Column 41, Lines 23-24]; and a corrective action mechanism, wherein if the request is a write request [Figure 1, # 218 & Column 41, Lines 31-35], the corrective action mechanism is configured to examine a read-only indicator within the object table entry [Figure 9, # 212, 214 & Column 41, Lines 25-29], and if the read-only indicator specifies that the object is a read-only object, to perform a corrective action to deal with the fact that the write request is directed to a read-only object [Figure 9, # 218 & Column 41, Lines 31-35].

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshioka et al. (US Patent # 6,324,634 B1) discloses an address translation table, which includes a data protection field. Weinreb et al. (US Patent # 5,649,139 A) discloses an object-oriented translation system for records in a database system that includes locking records for read/write protection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMM

MANO PADMANABHAN SUPERVISORY PATENT EXAMPLED

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